**AMENDMENTS TO THE DRAWINGS:**

The attached sheet of drawings includes new Figs. 1A and 1B, and adds to the original sheets of drawings.

Attachment: Additional Sheet showing Figs. 1A and 1B

## REMARKS

Claims 1-21 are pending. The Patent Office has rejected claims 1-18 and allowed claims 19-21. Claims 1, 7, 9, 17, and 18 have been amended for clarification in accordance with the Patent Office's suggestions at the bottom of page 3 of the Office Action mailed July 29, 2005. It is noted that claims 4, 5, 8, 12, 13, and 16 were not treated on the merits. It is presumed that the Patent Office considers these claims to contain allowable subject matter.

The drawings were objected to for not showing the structure of claims 3-5, 8, 11-13, and 16. New drawing figures 1A and 1B are being presented. Support for these drawing figures is found on page 6, lines 5-13. The specification, on page 6, lines 5-13, has accordingly been amended. It is respectfully submitted that new matter has been added.

The Patent Office rejected claims 4, 5, 8, 12, 13, and 16 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant's specification, on page 6, lines 6-10, discloses "this interconnect may in practice be provided in the form of a device driver in an adapter-based solution where the device driver communicates with an adapter (not shown) of the storage subsystem. Alternatively, the interconnect may communicate with a controller (not shown) of the storage subsystem." Thus, the adapter or a controller are part of the storage subsystem. Applicant asserts that one of ordinary skill would understand how an interconnect may be comprised of a device driver. Applicant respectfully requests that the Patent Office withdraw its rejection of claims 4, 5, 8, 12, 13, and 16, accordingly.

Applicant has disclosed it is known to provide a cache of subsystem configuration data. This provides a centralised point of reference for user information relating to the subsystem. It is known from U.S. patent no. 5,895,493 that such a system will gather information from various systems and provide a point for the user to access and obtain information about a group of systems (page 2, lines 1-5 of Applicant's disclosure).

However, this approach has the disadvantage(s) that the system of the referenced patent does not describe how this data is updated. It relies on the subsystems notifying the main cache of changes and updates and passing the data (page 2, lines 7-9 of Applicant's disclosure).

The preferred embodiment of this invention provides a way in which the configuration software running in the host can cache the results of the logical resource configuration discovery

transactions and hence re-use the same transaction data when applicable. The present invention is based on the realisation by the inventor that in general subsystem logical resources do not change, and that therefore the cache can be used in preference to "talking" to the subsystem to find out what it has in terms of logical resources. This results in greatly reduced user response times, and reduces the non-essential workload on the subsystem. In particular the preferred embodiment of this invention provides a method of cache update involving a 2-phase commit of the data (page 5, lines 9-17, of Applicant's disclosure).

The Patent Office rejected claims 1-3, 6, 7, 9-11, 14, 15, 17, and 18 under 35 U.S.C. 102(e) as being anticipated by Kavipurapu, U.S. Patent No. 6,584,546.

For a claim to be anticipated, each and every claim element must be disclosed by a reference (MPEP 2131) unless the claim element is an inherent feature.

Claim 1 recites "An apparatus for update of cache data in a storage system, the apparatus comprising a memory for storing data; a cache for storing data associated with the memory; at least one processor for preparing change data for updating the cache, the at least one processor comprising circuitry for **submitting a request for change to the memory, receiving a signal from the memory representative of completion of the request for change**; and **updating the cache with the change data in response to the signal indicating successful completion of the request for change**."

Claim 9 recites "A method for update of cache data in a storage system, the method comprising providing a memory holding data; providing a cache holding data associated with the memory; preparing change data for updating the cache; **submitting a request for change to the memory; receiving a signal from the memory representative of completion of the request for change**; and **updating the cache with the change data in response to the signal indicating successful completion of the request for change**."

Claim 17 recites "A computer program storage device readable by a machine and comprising executable computer program instructions for update of a cache in a storage system, the storage system comprising a memory holding data and a cache holding data associated with the memory, the instructions for performing the method of preparing change data for updating the cache; **submitting a request for change to the memory; receiving a signal from the memory representative of completion of the request for change**; and **updating the cache with the**

**change data in response to the signal indicating successful completion of the request for change.**"

Claim 18 recites "An apparatus for update of cache data in a storage system, the apparatus comprising memory means for holding data; cache means for holding data associated with the memory means; means for preparing change data for updating the cache means; means for **submitting a request for change to the memory** means; means for **receiving a signal from the memory means representative of completion of the request for change**; and means for **updating the cache means with the change data in response to the signal indicating successful completion of the request for change.**"

The Patent Office asserted "Regarding claim 1, Kavipurapu teaches an apparatus for update of cache date in a storage system, the apparatus comprising: a memory for storing data [Fig. 4; 401a, 401b]; a cache means for storing data associated with the memory [col. 4, lines 44-47]; at least one processor [Fig. 1] for preparing change data for updating the cache, the at least one processor comprising circuitry for submitting a request for change to the memory [Tag search], receiving a signal from the memory representative of the completion of the request for change [Tag hit response], and updating the cache with the change data [write operation] in response to the signal indicating successful completion of the request for change [col. 6, line 54 – col. 7, line 19]."

Kavipurapu discloses (column 6, line 52, through column 7, line 19) as follows:

The WRITE protocol used by the controller is shown in FIG. 9. In the first write scenario:
1) Processor Write.fwdarw.Bank 2 Search (**Tag Search**).fwdarw.Tag Hit.fwdarw.Overwrite the Tag that matches with the same Tag in the Tag directory for Bank 2 and "Set" the valid bit. Overwrite the data corresponding to the Tag entry in Bank 2.

To maintain coherency of data, Bank 1 is also searched and the valid bit is changed to "Dirty" if there is a Tag hit in the Tag directory for Bank 1. The data are not overwritten such that the entry at the line number corresponding to this Tag value is free to be overwritten in the next write cycle from a lower level memory prefetch, fetch, or an

update from Bank 2. The processor write pointer, which is separate from a memory write pointer, is not updated and points to the line with first "Dirty" valid bit in Bank 2, or the first line in Bank 2, otherwise if no Dirty bit is set. On the first Tag hit on a processor write, and on subsequent processor writes, the processor write pointer gets updated by 2, so as not to overwrite data from Address `A.`

The processor write pointer is only used as a replacement instrument in case of a Tag miss as shown in scenario 2:

2) Processor Write.fwdarw.Bank 2 Search (Tag Search).fwdarw.Tag Miss.fwdarw.Overwrite Tag entry in Tag directory for Bank 2 at the index that will be equal to the processor write pointer with new address Tag generated by the processor. Replace the data in the line that corresponds to the index of the processor write pointer. To avoid coherency problems check the Bank 1 Tags in the Tag directory entries for Bank 1. (Since there might be a Tag match in Bank 1 even though there is Tag miss in Bank 2 this step is necessary.) If there is a Tag hit in the Tag directory for Bank 1 then set the valid bit to "Dirty" If there is no match then the directory entries for Bank 1 are left unchanged.

Although Kavipurapu discloses that the cache may be written to, Kavipurapu does not disclose "**submitting a request for change to the memory**" (e.g., to the controller), "**receiving a signal from the memory representative of completion of the request for change,**" or "updating the cache with change data **in response to the signal indicating successful completion of the request for change.**" Tag search is not the submission of a request for a change to memory, but involves a directive or instruction from the processor to the cache to search for a tag in a bank of cache. If a hit is found in the Bank 1 tag directory, the Bank 1 of the mirrored memory is preferentially accessed (column 7, lines 45-47). Kavipurapu does not disclose "receiving a signal from the memory representative of completion of the request for change" since Kavipurapu does not disclose or suggest what determines that the controller initiates a write to cache. Although Kavipurapu discloses setting a bit in accordance with a write operation to a cache bank, Kavipurapu does not disclose "updating the cache with change data **in response to the signal indicating successful completion of the request for change.**" Thus,

Kavipurapu does not anticipate (or make obvious) claims 1-3, 6, 7, 9-11, 14, 15, 17, or 18.

Claims 2 and 10 recite "wherein the data comprises configuration data." The Patent Office asserted (page 5, lines 13-14) "Regarding claim 2, Kavipurapu teaches wherein the data comprises configuration data [data configured for associative cache scheme; col. 3, lines 3-13]." On the contrary, Kavipurapu discloses "in a fully associative cache scheme, a block of instructions or data can be placed anywhere within the cache" (col. 3, lines 6-8). Thus, claims 2 and 10 are not anticipated by Kavipurapu for this additional reason.

Claims 4 and 12 recite "wherein the memory is comprised in a disk adapter." Claims 5 and 13 recite "wherein the memory is comprised in a disk controller." Kavipurapu does not disclose that the memory is comprised in a disk adapter or comprised in a disk controller. Thus, Kavipurapu does not anticipated claims 4, 5, 12, and 13.

Claims 7 and 15 recite "wherein the interconnect is also arranged to communicate transaction data." It appears that Kavipurapu is only concerned with the transfer of instructions or data to cache (column 3, lines 3-12) and not with transaction data. It is respectfully submitted that claims 7 and 15 are allowable for this additional reason.

The Patent Office is respectfully requested to reconsider and remove the rejections of the claims 1-3, 6, 7, 9-11, 14, 15, 17, and 18 under 35 U.S.C. 102(e) based on Kavipurapu, and to allow all of the pending claims 1-21 as now presented for examination. An early notification of the allowability of claims 1-21 is earnestly solicited.

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Respectfully submitted:

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